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A Power-up Circuit for a PC Card

This invention relates to a power-up circuit for a PC card. The invention also relates to a method of supplying current to a PC card.

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A PC card, or PCMCIA card, is a peripheral module which is commonly used in conjunction with modern personal computers (PCs). In its most common form, a PC card comprises a printed circuit board located in a slim casing, which can be plugged into the peripheral port of a PC in order to perform a particular function. As an example, a PC card might include some memory ICs which allow the PC to store data on a removable card to take the place of a floppy disk. As a further example, a PC card might include a modem for allowing the computer to access the Internet via a telephone line or over a wireless communications network. A PC Card generally comprises a plurality of sub-circuits, or sub-modules.

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The electrical standards applicable to PC card devices are defined by the so-called PCMCIA specifications. These specifications state that the total current taken by a PC card, when power is initially applied to the card (i.e. at the "power-up" phase), should be less than a specified limit. In the case of PC cards operating from 3 volt and 5 volt power sources, the respective limits are 70 mA and 100 mA. After the initial power-up phase, the PCMCIA specifications permit the current to exceed this limit. This is referred to as the "operational phase" of the PC card.

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In conventional PC Cards, it is quite common for the current level to exceed the PCMCIA standard during the power-up phase. This is generally caused by the presence, in the sub-circuits, of reservoir capacitors, which are provided to smooth the current drawn by each sub-circuit during the operational phase. When power is initially applied to a sub-circuit, the effect of its reservoir capacitor is such that a large pulse of current is drawn from the source as the source voltage is established. Since there are usually two or more sub-circuits on a PC card, such multiple current pulses can cause the total current to exceed the PCMCIA standard.

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According to a first aspect of the present invention, there is provided a power-up circuit for a PC card having a plurality of sub-circuits, comprising means for controlling the amount of current initially taken by at least one of the sub-circuits, such that the total
5 current taken by the plurality of sub-circuits does not exceed a predetermined threshold value at a given instant in time.

Preferably, the current-controlling means is such as to control the sequence in which the plurality of sub-circuits initially take current from a source. In this way, by effectively
10 powering-up each individual sub-circuit separately and in a particular sequence, the total amount of current drawn at a particular instant in time can be kept well within the level specified by the PCMCIA standard.

In a preferred embodiment, the current-controlling means is arranged such that the
15 sub-circuit drawing the least d.c. current is turned on first, with the sub-circuit drawing the most d.c. current being turned on last. The current-controlling means may be provided in the form of delay elements, or may be provided as a software-controlled microprocessor. The current-controlling means may further include means arranged to control the rate at which one or more of the sub-circuits initially takes current from the
20 source.

Since the PCMCIA standard states that, after the "power-up" phase, the current level may exceed the predetermined threshold value, then the power-up circuit may be further arranged so that, after an initialisation time period, the magnitude of the total current
25 taken by the sub-circuits is allowed or caused to exceed the predetermined threshold value.

With suitable circuit design, it is possible to provide a power-up circuit which meets the PCMCIA standards, as outlined above.

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According to a second aspect of the present invention, there is provided a method of supplying current to a PC card having a plurality of sub-circuits, wherein during a

power-up phase, the current supplied to at least one sub-circuit is controlled so that the total current supplied to the plurality of sub-circuits, at a given instant in time, does not exceed a predetermined threshold value.

- 5 Preferred features of the method are specified in the accompanying claims.

The invention will now be described, by way of example, with reference to the accompanying drawings, in which:

- 10 Figure 1 shows a block diagram of a PC card circuit, incorporating power-up circuitry constructed in accordance with the invention;

Figure 2 is a graph showing individual and total current values taken by first and second sub-circuits of the PC card circuit of Figure 1; and

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Figure 3 is a functional block diagram showing the procedural operating steps during the power-up and operational phases of the PC card operation.

- Figure 1 shows a PC card circuit 1 comprising two sub-circuits 2, 7. The sub-circuit 2
20 comprises a radio circuit 3 and a reservoir capacitor 5 for smoothing the current drawn by the radio circuit. The sub-circuit 7 is a processor sub-circuit which is connected by its output terminal to the gate terminal of a field-effect transistor (FET) switch 15. The FET switch 15 bridges a resistor 13 which provides a high impedance path to the capacitor 5. Accordingly, the FET switch 15 has its drain terminal connected to the
25 radio circuit 3, and its source terminal to a port 16. A delay circuit is provided at the input to the processor sub-circuit 7, the delay circuit 11 being connected in serial with voltage regulation circuitry 9. The delay circuit 11 is connected to the port 16.

- Power is provided to the PC card, via a personal computer (not shown), to which the
30 PC card is attached, by means of port 16.

In operation, the PC card circuit 1 works in two main phases. In the first phase, known as the "power-up" phase, the sub-circuits 2, 7 receive power from the source, and the PC card is required to undergo various initialisation and detection stages. The main function of the processor sub-circuit 7 is to communicate with the PC processor during the initialisation and detection stages, and also during the main operating phase of the PC card. In the power-up phase, the total current taken by the sub-circuits 2, 7 must also be within the PCMCIA specified limits. In the case of a 3 volt PC card, this limit is 70 mA, whilst for a 5 volt PC card, this limit is 100 mA. After the power-up phase, the PC card enters the "operational" phase, wherein the PC card operates as a radio data transceiver. In the operational phase, the total current drawn may exceed the specified limits, whilst still complying with the PCMCIA specification.

At the time when power is input to the PC card circuit 1, i.e. at the start of the power-up phase, the radio circuit 3 takes very little d.c. current from the source. Whilst the reservoir capacitor 5 will take no d.c. current in the steady state condition, it will, however, take considerable current when initially charging in the power-up phase. In order to reduce this effect, a high impedance path is provided by the resistor 13. The RC arrangement of the capacitor 5 and the resistor 13 allows the capacitor to charge at a controlled rate. The resistor 13 is bridged by the FET switch 15 which acts as a bypass switch in the operational phase, as will be explained below.

At the start of the power-up phase, no current is drawn by the processor sub-circuit 7 because of the delay circuit 11. The delay circuit is required in order for the PC card circuit 1 to meet the PCMCIA specification, as will be explained in detail below. The delay circuit 11 can take the form of a reset generator IC, a simple RC network, or even a software-controlled microprocessor. A software-controlled microprocessor is particularly useful in that delays can be conveniently set for many sub-circuits, and they may be easily adjusted. After a predetermined time period set by the delay circuit 11, current is drawn by the processor sub-circuit 7 through the voltage regulating circuitry 9. The processor sub-circuit 7 takes a significant d.c. current. In addition, there are some smoothing capacitors (not shown) in the processor sub-circuit 7 which take additional current when they initially charge. By delaying the initialisation of the

processor sub-circuit 7 in the power-up phase, it is ensured that the total current taken by the two sub-circuits will never exceed the predetermined threshold. This will be understood better by examining the graph of Figure 2.

- 5 Figure 2 is a graph illustrating the amount of current taken by each sub-circuit 2, 7 of the PC card circuit 1 during the course of the power-up phase. On the graph, the current taken by the radio sub-circuit 2 is represented by the broken trace 17, whilst the current taken by the processor sub-circuit 7 is represented by the broken trace 18. The bold line 19 represents a trace of the total current taken by the two sub-circuits at that particular instant in time. The predetermined current threshold is represented by the horizontal line, I_{Limit} .

- 15 It will be seen that, at the start of the power-up phase ($t = T1$), the current taken by the radio sub-circuit 2 shows a large pulse on the graph (due to the charging of the large capacitor 5). Peak current occurs at point A. As the capacitor 5 begins to charge, the current taken by the sub-circuit 2 decays exponentially with a time constant equal to the impedance multiplied by the capacitance. The processor sub-circuit 7 draws no current at this time due to the delay circuit 11.

- 20 The processor sub-circuit begins to draw current at $t = T2$, at which point there is a further current pulse due to the fact that the processor takes a significant d.c. current and has some capacitance associated with it. The peak amount of current taken is indicated by point B. It is seen that this current value, when added to the current taken by the radio sub-circuit 2 at this instant in time, results in the total current value C. As the capacitors (not shown) associated with the processor sub-circuit 7 charge, the amount of current taken by this sub-circuit decreases at an exponential rate.

- 30 It is seen that, by sequencing the time at which each sub-circuit 2, 7 begins to take current, the total amount of current never exceeds the current threshold I_{Limit} . The sequence in which the sub-circuits 2, 7 are 'turned-on' (i.e. when they draw current in the power-up phase) is such that the sub-circuit drawing the least steady-state d.c. current is turned-on first, with the sub-circuit drawing the most steady-state d.c. current

being turned-on last. In effect, the timing of the sequence is arranged such that the current charging the capacitor 5 in the radio sub-circuit 3 is allowed to decay to a sufficient level so that the peak current of the processor sub-circuit 7 does not exceed the current threshold I_{Limit} . In this way, it is possible to accommodate the sub-circuits without exceeding the current threshold. This order of sequencing is particularly advantageous as the number of sub-circuits increases.

After a predetermined time period, depending on the operation of the PC (for example 2 to 3 seconds), the PC card circuit 1 operates in the operational phase. In this mode, the PCMCIA specification specifies that the total current taken need not be within the predetermined threshold level I_{Limit} . Indeed, to ensure proper operation of particular sub-circuits, such as the radio sub-circuit 3, it is preferable that the current taken does exceed the I_{Limit} during the operational phase. In order to accommodate this feature, and to terminate the power-up phase, the processor sub-circuit 7 outputs a signal to turn-on the FET 13. This acts to bypass the resistor 13, and thus allows more current to pass to the capacitor 5. Accordingly, higher currents may be taken by the radio sub-circuit 3, from the source, during the operational phase.

Finally, with reference to Figure 3, there is detailed the typical procedural steps associated with the operation of a PC card incorporating the above described PC card circuit 1.

Initially, at block 21, the PC card is inserted into a suitable port of a PC. When the PC is turned-on, the PC detects the card insertion (block 28), and power is supplied to the PC card as the power-up phase commences. As mentioned above, the capacitor 5 will begin to charge, resulting in a current pulse which is limited by the impedance of R1 13 (block 22). After the delay period has passed, the processor sub-circuit 7 begins to power-up (block 23). After this, the processor of the PC card is reset, and the Card Information Structure (CIS) data is initialised by the processor (blocks 24 and 25). Once the CIS data is initialised, the PC operates to detect and identify the card type (block 29). In order to terminate the power-up phase, and to commence the operational phase, the FET switch 15 is enabled to bypass the resistor 13, and more current is

allowed to flow to the radio sub-circuit 3 (block 26). In the operational phase, the card is fully functional, and operates with the radio sub-circuit 3 to act as a mobile data transmitting and receiving device (block 27). Having identified the card type, the PC is fully capable of communicating with the PC card (block 30).

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It will be appreciated that, although only two sub-circuits are referred to in this particular embodiment, the invention provides a way in which more than two sub-circuits may be incorporated on a PC card such that the PCMCIA specification on power-up current levels can be met.

Claims

1. A power-up circuit for a PC card having a plurality of sub-circuits, the power-up circuit comprising means for controlling the amount of current initially taken by at least one of the sub-circuits, such that the total current taken by the plurality of sub-circuits does not exceed a predetermined threshold value at a given instant in time.
2. A power-up circuit according to claim 1, wherein the current-controlling means is such as to control the sequence in which the plurality of sub-circuits initially take current from a source.
3. A power-up circuit according to claim 2, wherein the current-controlling means is a delay circuit which prevents current being taken, by at least one of the sub-circuits, for a predetermined time period.
4. A power-up circuit according to claim 3, wherein the delay circuit comprises a reset generator IC, an RC network, or a software-controlled microprocessor.
5. A power-up circuit according to any of claims 2 to 4, wherein the current-controlling means is arranged such that the sub-circuit drawing the least d.c. current is turned on first, with the sub-circuit drawing the most d.c. current being turned on last.
6. A power-up circuit according to any of claims 2 to 5, wherein the current-controlling means further includes means to control the rate at which at least one sub-circuit initially takes current from a source.
7. A power-up circuit according to any preceding claim, wherein the PC card operates with a supply voltage in the region of 3 volts, and wherein the predetermined first threshold value is 70 mA.

8. A power-up circuit according to any of claims 1 to 6, wherein the PC card operates with a supply voltage in the region of 5 volts, and wherein the predetermined first threshold value is 100 mA.
- 5 9. A power-up circuit according to any preceding claim, further arranged such that, after an initialisation time period, the magnitude of the total current taken by the sub-circuits of the PC card is allowed to exceed the predetermined first threshold value.
- 10 10. A method of supplying current to a PC card having a plurality of sub-circuits, the method comprising the step of controlling the current supplied to at least one sub-circuit so that the total current supplied to the plurality of sub-circuits, at a given instant in time, does not exceed a predetermined first threshold value.
- 15 11. A method according to claim 10, further controlling the sequence in which current is initially supplied to the plurality of sub-circuits.
- 20 12. A method according to claim 11, wherein the sub-circuit drawing the least d.c. current is turned on first, and wherein the sub-circuit drawing the most d.c. current is turned on last.
- 25 13. A method according to claim 11 or claim 12, further comprising controlling the rate at which at least one of the plurality of sub-circuits takes current from a source.
14. A method according to any of claims 10 to 13, wherein, after the power-up phase, the PC card operates in an operational phase in which the total current supplied to the plurality of sub-circuits is caused to exceed the predetermined first threshold value.

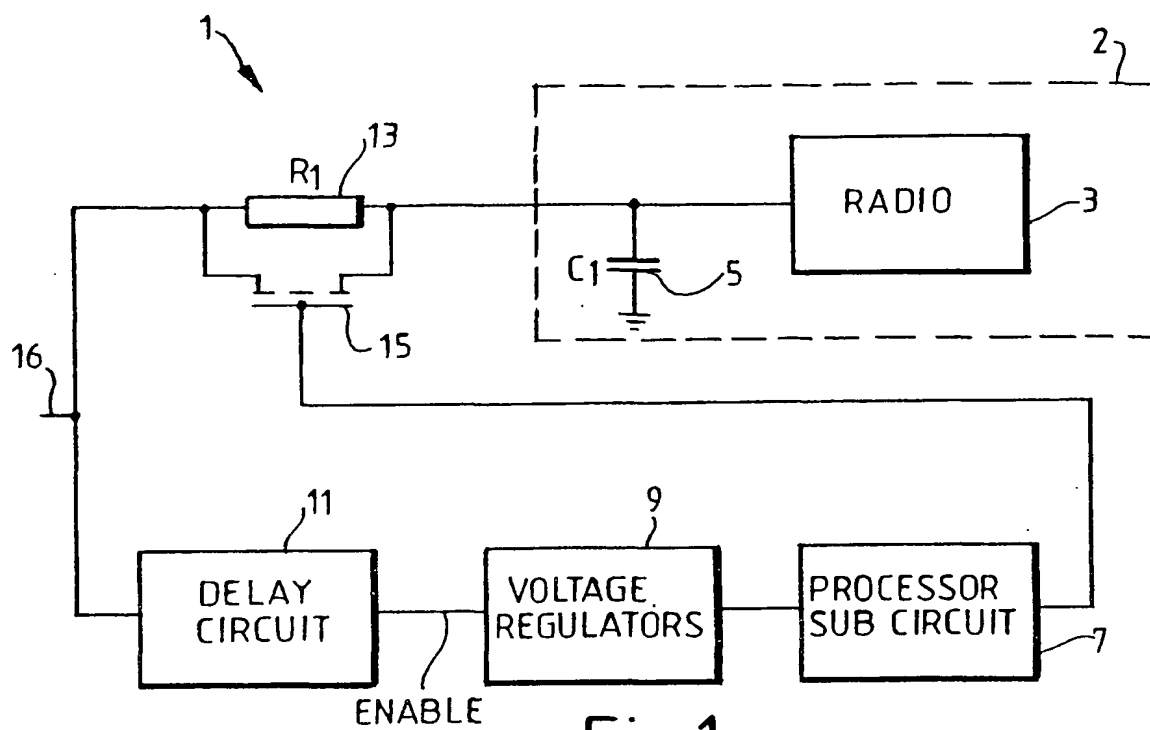


Fig.1.

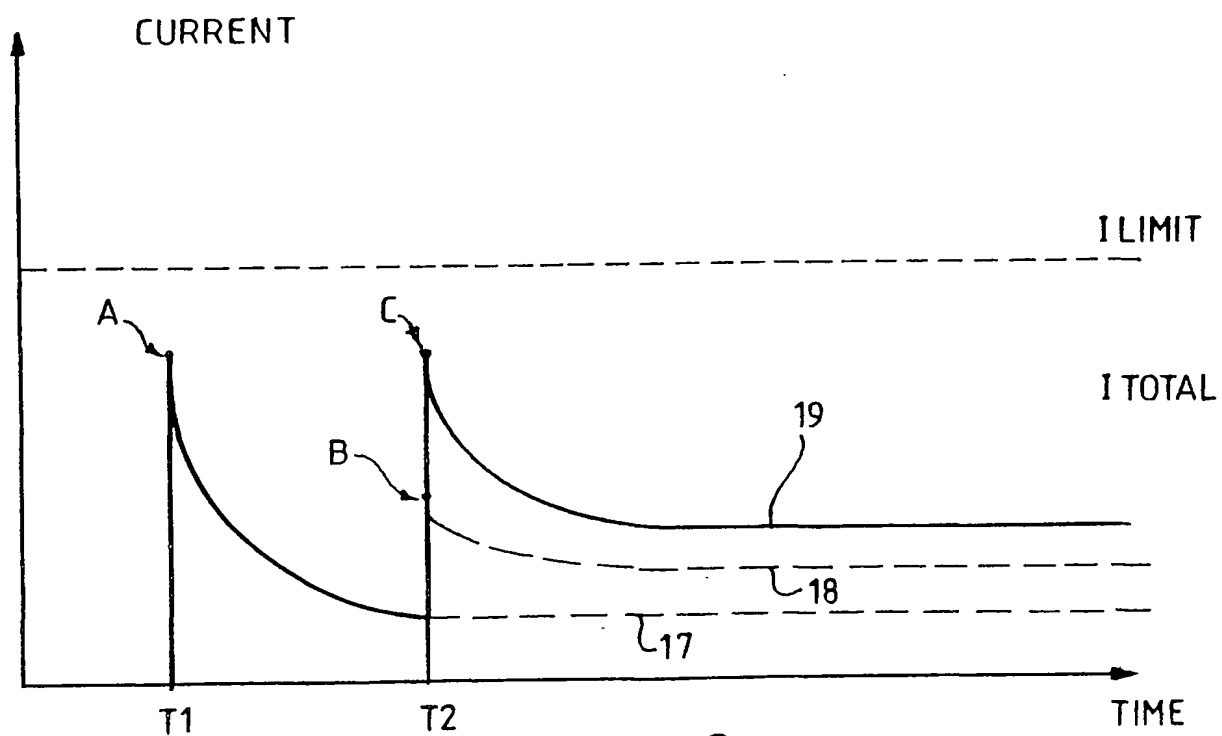


Fig.2.

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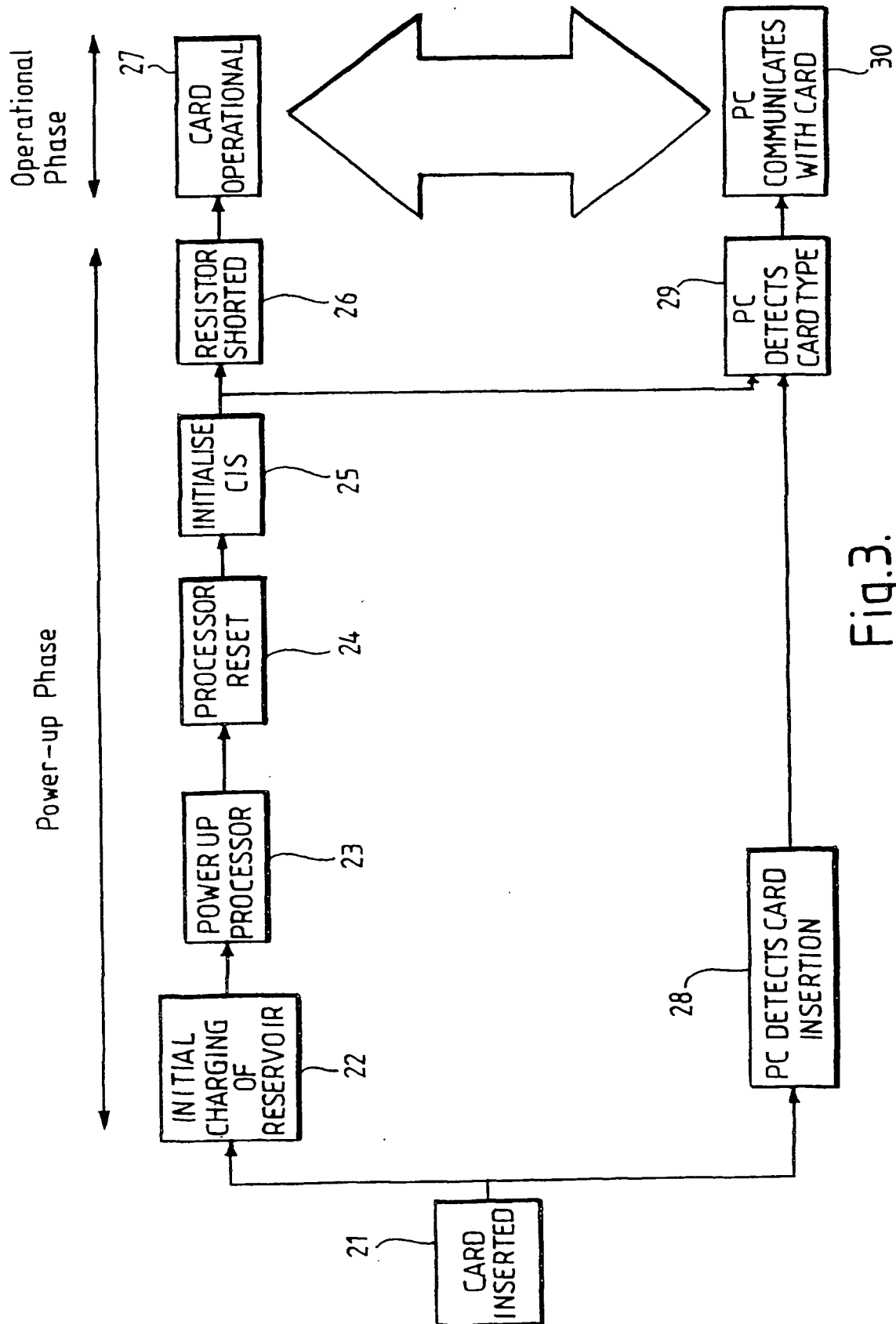


Fig.3.

INTERNATIONAL SEARCH REPORT

International Application No

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A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 G06F1/28 G06F1/26 G06F1/30

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 729 062 A (SATO SHUNJI) 17 March 1998 (1998-03-17) the whole document	1-14
X	US 5 675 467 A (HONDA SHIGERU ET AL) 7 October 1997 (1997-10-07) abstract column 2, line 55 -column 3, line 20 column 4, line 10 -column 5, line 25; figures 1A-C column 10, line 9 -column 11, line 5; figure 2	1,7,8,10
A	---	2-4,6, 11,13
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European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx 31 651 epo nl.
Fax: (+31-70) 340-3016

Authorized officer

Davenport, K

INTERNATIONAL SEARCH REPORT

International Application No

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	<p>EP 0 814 399 A (ARCHOS) 29 December 1997 (1997-12-29) abstract column 1, line 1 -column 4, line 37 -----</p>	1,7,8,10

INTERNATIONAL SEARCH REPORT

Information on patent family members

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Patent document cited in search report		Publication date		Patent family member(s)	Publication date
US 5729062	A	17-03-1998	JP	2830786 B2	02-12-1998
			JP	9050333 A	18-02-1997
US 5675467	A	07-10-1997	JP	8152948 A	11-06-1996
EP 0814399	A	29-12-1997	FR	2750228 A1	26-12-1997
			EP	0814399 A1	29-12-1997
			US	6044472 A	28-03-2000

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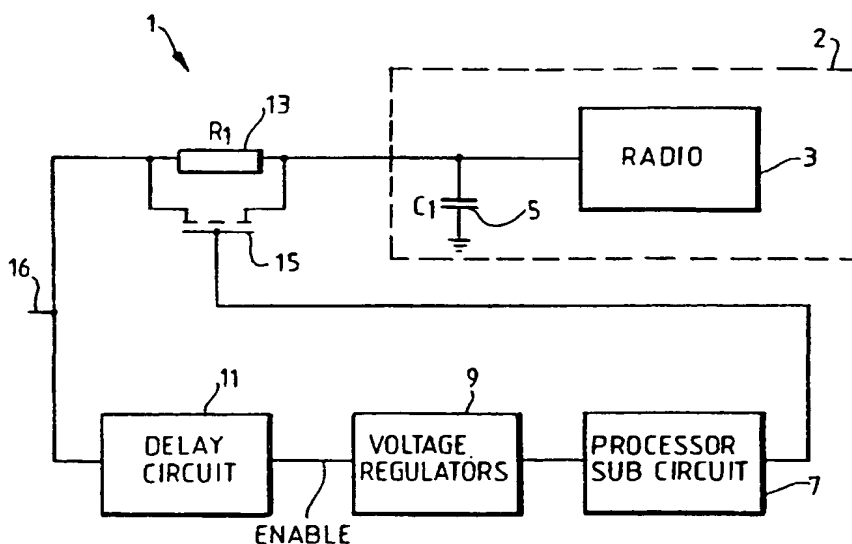
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- (72) Inventor; and
(75) Inventor/Applicant (*for US only*): APPLETON, Ian, Kenneth [GB/GB]; 35 Willian Way, Letchworth, Hertfordshire SG6 2HQ (GB).
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(54) Title: A POWER-UP CIRCUIT FOR A PC CARD



(57) Abstract: A PC card (1) comprises a power-up circuit for controlling the power-up sequence of two sub-circuits (2, 7) of the PC card. The first sub-circuit (7) is a processor sub-circuit for communicating with a PC, to which the PC card is attached. The second sub-circuit (2) is a radio. When power is initially applied to the PC card (1), the radio sub-circuit (2) initially draws a large amount of current. A delay circuit (11) of the power-up circuit prevents current being taken by the processor sub-circuit (7), thereby ensuring that the total current taken by the PC card (1) does not exceed a predetermined current level. After a predetermined time period, the current taken by the radio sub-circuit (2) decays and current is allowed to be taken by the processor sub-circuit (7). By sequencing the power-up of the sub-circuits (2, 7) in this way, the total current taken by the PC card (1) can be kept within the PCMCIA specified limits during the so-called power-up phase.

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